



Automotive LPDDR5/LPDDR5X SDRAM

MT62F768M32D2, MT62F1536M32D4, MT62F3G32D8

Features

- **Architecture**
 - 17.1 GB/s maximum bandwidth per channel
 - Frequency range: 1067–5 MHz (data rate range per pin: 8533–40 Mb/s with WCK:CK = 4:1)
 - Selectable CKR (WCK:CK = 2:1 or 4:1)
- **LPDDR5X data interface**
 - Single x16 channel/die
 - Double-data-rate command/address entry
 - Differential command clocks (CK_t/CK_c) for high-speed operation
 - Differential data clocks (WCK_t/WCK_c)
 - Differential read strobe (RDQS_t/RDQS_c)
 - 16n-bit or 32n-bit prefetch architecture
 - Command-selectable burst lengths (BL = 16 or 32) in bank group or 16-bank modes
 - Background ZQ calibration/command-based ZQ calibration
 - Link protection (link ECC) support
 - Partial-array self refresh (PASR) and partial-array auto refresh (PAAR) with segment mask
- **Ultra-low-voltage core and I/O power supplies**
 - $V_{DD1} = 1.70\text{--}1.95\text{V}$; 1.80V TYP
 - $V_{DD2H} = 1.01\text{--}1.12\text{V}$; 1.05V TYP
 - $V_{DD2L} = V_{DD2H}$ or $0.87\text{--}0.97\text{V}$; 0.90V TYP
 - $V_{DDQ} = 0.50\text{V}$ TYP or 0.30V TYP (ODT off only)
- **I/O characteristics**
 - Interface-LVSTL 0.5/0.3
 - I/O type: Low-swing single-ended, V_{SS} terminated
 - V_{OH} -compensated output drive
 - Programmable V_{SS} on-die termination (ODT)
 - Non target ODT support
 - DVFSQ support
- **Low-power features**
 - DVFSC: Dynamic voltage frequency scaling core
 - Single-ended CK, single-ended WCK, and single-ended RDQS
 - Data copy
 - Write X

Options

- **Operating Voltage**
 - $V_{DD1}/V_{DD2H}/V_{DD2L}/V_{DDQ}/V_{DDQ}(\text{ODT off only}): 1.8\text{V}/1.05\text{V}/0.9\text{V}/0.5\text{V}/0.3\text{V}$
- **Array configuration**
 - 768 Meg x 32 (768M16 x 2Ch x 1R) 768M32
 - 1536 Meg x 32 (768M16 x 2Ch x 2R) 1536M32
 - 3 Gig x 32 (1536M16 x 2Ch x 2R) 3G32
- **Device configuration**
 - 2 die in package (768M16 x 2 die) D2
 - 4 die in package (768M16 x 4 die) D4
 - 8 die in package (1536M8 x 8 die) D8
- **FBGA RoHS-compliant, "green" package**
 - 315-ball TFBGA DS
12.4mm x 15.0mm (TYP)
Seated height 1.1mm (MAX)
 - 315-ball LFBGA DV
12.4mm x 15.0mm (TYP)
Seated height 1.3mm (MAX)
- **Speed grade, cycle time (t^1 WCK)**
 - 8533 Mb/s -023
 - 7500 Mb/s -026
- **Functional safety features**
 - Micron safety features enabled
 - Suitable for meeting random HW metrics up to ASIL D F
- **Automotive and functional safety**
 - AEC-Q100 A¹
 - PPAP
 - ISO 26262 ASIL D compliant development
 - FMEDA (ISO 26262-5:2018, cl. 8, 9)
 - Safety manual
- **Operating temperature**
 - $-40^\circ\text{C} \leq T_C \leq +95^\circ\text{C}$ IT
 - $-40^\circ\text{C} \leq T_C \leq +105^\circ\text{C}$ AT
 - $-40^\circ\text{C} \leq T_C \leq +125^\circ\text{C}$ UT²
- **Revision** :B

- Notes: 1. For functional safety documentation, contact a Micron sales representative.
2. Based on automotive usage model. Contact a Micron sales representative with questions.



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Part Number Ordering Information

Part Number Ordering Information

Figure 1: Part Number Chart

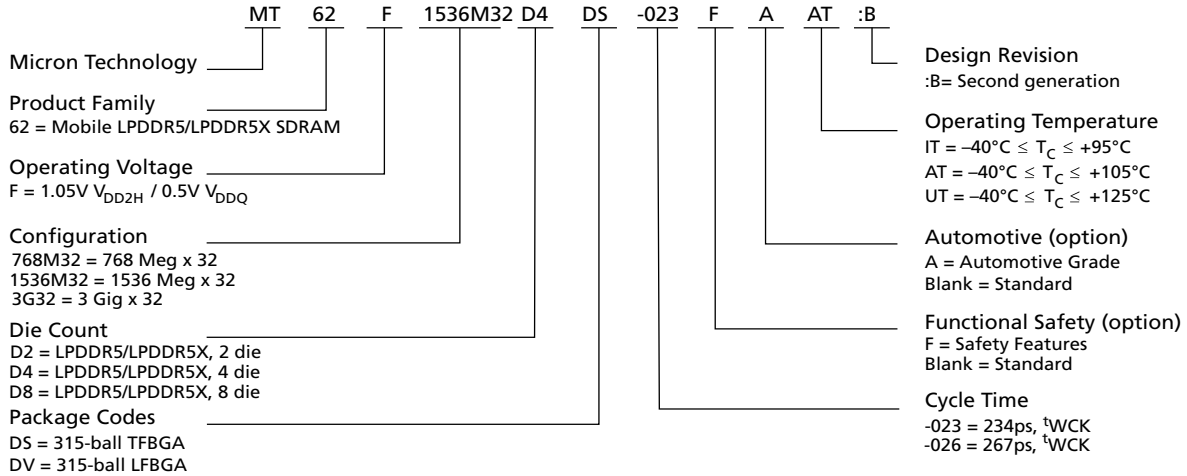


Table 1: Part Number List

Part Number	Total Density	Data Rate per Pin
MT62F768M32D2DS-023 AIT:B	3GB (24Gb)	8533 Mb/s
MT62F768M32D2DS-023 AAT:B		
MT62F768M32D2DS-023 AUT:B		
MT62F768M32D2DS-023 FAAT:B		
MT62F1536M32D4DS-023 AIT:B	6GB (48Gb)	
MT62F1536M32D4DS-023 AAT:B		
MT62F1536M32D4DS-023 AUT:B		
MT62F1536M32D4DS-023 FAAT:B		
MT62F3G32D8DV-023 AIT:B	12GB (96Gb)	
MT62F3G32D8DV-023 AAT:B		
MT62F3G32D8DV-023 AUT:B		
MT62F3G32D8DV-023 FAAT:B		
MT62F1536M32D4DS-026 AIT:B	6GB (48Gb)	7500 Mb/s
MT62F1536M32D4DS-026 AAT:B		
MT62F3G32D8DV-026 AIT:B	12GB (96Gb)	
MT62F3G32D8DV-026 AAT:B		

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Part Number Ordering Information

LPDDR5/LPDDR5X Data Sheet List

This data sheet only describes the product specifications that are unique to the Micron devices listed in Table 1.

For general LPDDR5/LPDDR5X specifications, please refer to the data sheets below.

- General LPDDR5/LPDDR5X Specifications 1: Mode Registers
- General LPDDR5/LPDDR5X Specifications 2: AC/DC and Interface Specifications
- General LPDDR5/LPDDR5X Specifications 3: Features and Functionalities



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315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Important Notes and Warnings

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General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQs collectively, unless specifically stated otherwise.

RDQS, CK, and WCK should be interpreted as RDQS_t, RDQS_c, CK_t, CK_c, and WCK_t, WCK_c respectively unless specifically stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[6:0].

V_{REF} indicates $V_{REF(CA)}$ and $V_{REF(DQ)}$.

Complete functionality is described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.

Any functionality not specifically stated herein is considered undefined, illegal, is not supported, and will result in unknown operation.



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Functional Safety Notes

Functional Safety Notes

This automotive LPDDR5/LPDDR5X DRAM product family has been developed according to ISO 26262:2018 requirements to provide a level of systematic fault coverage that allows its use in systems targeting up to ASIL D compliance.

This LPDDR5/LPDDR5X DRAM contains several new functional safety features that operate within the JEDEC LPDDR5/LPDDR5X protocols (commands, timings, and so forth) and are made available to the integrator on “F” parts (see Part Number Ordering Information). The specification addendum governing these functional safety features is available under NDA. This LPDDR5/LPDDR5X DRAM may operate as a standard JEDEC LPDDR5/LPDDR5X DRAM only, or as a standard JEDEC LPDDR5/LPDDR5X DRAM specifically designed to include functional safety features to communicate fault detection (only available on “F” parts). Additional support may be available to customers who need to integrate Micron’s products in their functional safety-related applications. This support may include Safety Analysis Report, reporting FMEDA results and metrics, Safety Manual and Pin FMEA Report, providing guidelines and instructions for using Micron products in safety-related applications.

Contact a Micron sales representative to initiate the process required to obtain the functional safety documentation.



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Device Configuration

Device Configuration

Table 2: Die Organization in the Package

Die Organization	768M32 (24 Gb/package)	1536M32 (48 Gb/package)	3G32 (96 Gb/package)
Channel A	x16 mode × 1 die	–	–
Channel B	x16 mode × 1 die	–	–
Channel A, rank 0	–	x16 mode × 1 die	–
Channel B, rank 0	–	x16 mode × 1 die	–
Channel A, rank 1	–	x16 mode × 1 die	–
Channel B, rank 1	–	x16 mode × 1 die	–
Channel A, rank 0, DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 1, DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 0, DQ[7:0]	–	–	x8 mode × 1 die
Channel B, rank 1, DQ[7:0]	–	–	x8 mode × 1 die
Channel A, rank 0, DQ[15:8]	–	–	x8 mode × 1 die
Channel A, rank 1, DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 0, DQ[15:8]	–	–	x8 mode × 1 die
Channel B, rank 1, DQ[15:8]	–	–	x8 mode × 1 die

Note: 1. Refer to the Package Block Diagram section in this data sheet.

Table 3: Die Addressing

Description	768M32 (24Gb/package), 1536M32 (48Gb/package)			3G32 (96 Gb/package)		
	BG mode	16B mode	8B mode	BG mode	16B mode	8B mode
Density per die	12Gb			12Gb		
Bits	12,884,901,888			12,884,901,888		
Configuration	48Mb × 16 DQ × 4 banks × 4BG	48Mb × 16 DQ × 16 banks	96Mb × 16 DQ × 8 banks	96Mb × 8 DQ × 4 banks × 4BG	96Mb × 8 DQ × 16 banks	192Mb × 8 DQ × 8 banks
Number of banks	4	16	8	4	16	8
Number of bank groups	4	1	1	4	1	1
Array prefetch bits	256	256	512	128	128	256
Rows per bank	49,152			98,304		
Columns	64			64		
Page size (bytes)	2048	2048	4096	1024	1024	2048
Native burst length	16	16	32	16	16	32
Number of I/Os	16			8		



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Refresh Requirement Parameters

Table 3: Die Addressing (Continued)

Description	768M32 (24Gb/package), 1536M32 (48Gb/package)			3G32 (96 Gb/package)		
	BA[1:0]	BA[3:0]	BA[2:0]	BA[1:0]	BA[3:0]	BA[2:0]
Bank address	BA[1:0]	BA[3:0]	BA[2:0]	BA[1:0]	BA[3:0]	BA[2:0]
Bank group address	BG[1:0]	–	–	BG[1:0]	–	–
Row address	R[15:0] (R14 = 0 when R15 = 1)			R[16:0] (R15 = 0 when R16 = 1)		
Column address	C[5:0]			C[5:0]		
Burst address	B[3:0]	B[3:0]	B[4:0]	B[3:0]	B[3:0]	B[4:0]
Burst starting address boundary	128-bit			128-bit		

- Notes: 1. Refer to the SDRAM Addressing section in General LPDDR5/LPDDR5X Specifications 3.
2. Refer to the Speed Grades and Effective Burst Length in General LPDDR5/LPDDR5X Specifications 3.

Refresh Requirement Parameters

Table 4: Refresh Requirement Parameters

Parameter	Symbol	12Gb Die		Unit
		BG and 16B Mode	8B Mode	
REFRESH cycle time (all banks)	t_{RFCab}	280	280	ns
REFRESH cycle time (per bank)	t_{RFCpb}	140	140	ns
Per bank refresh to per bank refresh time (different bank)	$t_{PBR2PBR}$	90	90	ns
Per bank refresh to ACTIVATE command time (different bank)	$t_{PBR2ACT}$	7.5	10	ns

- Note: 1. This table only describes refresh parameters that are density dependent. Refer to Refresh Requirement section in General LPDDR5/LPDDR5X Specifications 3 for all refresh parameters.

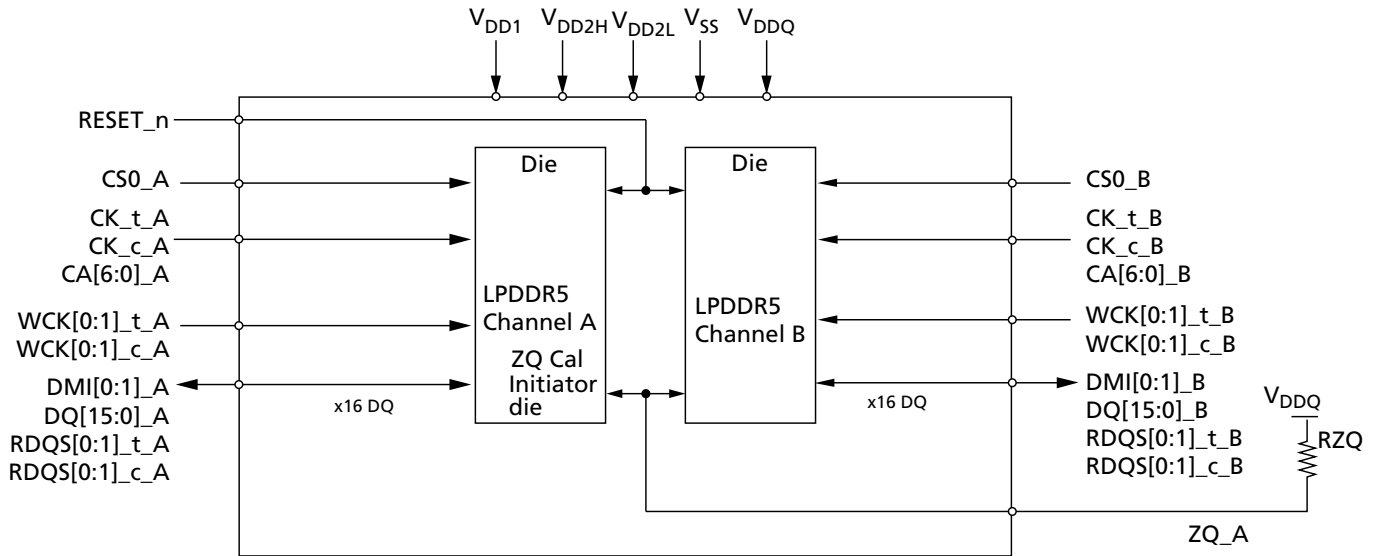


315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Package Block Diagrams

Package Block Diagrams

Dual Die, Dual Channel, Single Rank

Figure 2: Dual Die, Dual Channel, Single Rank Package Block Diagram

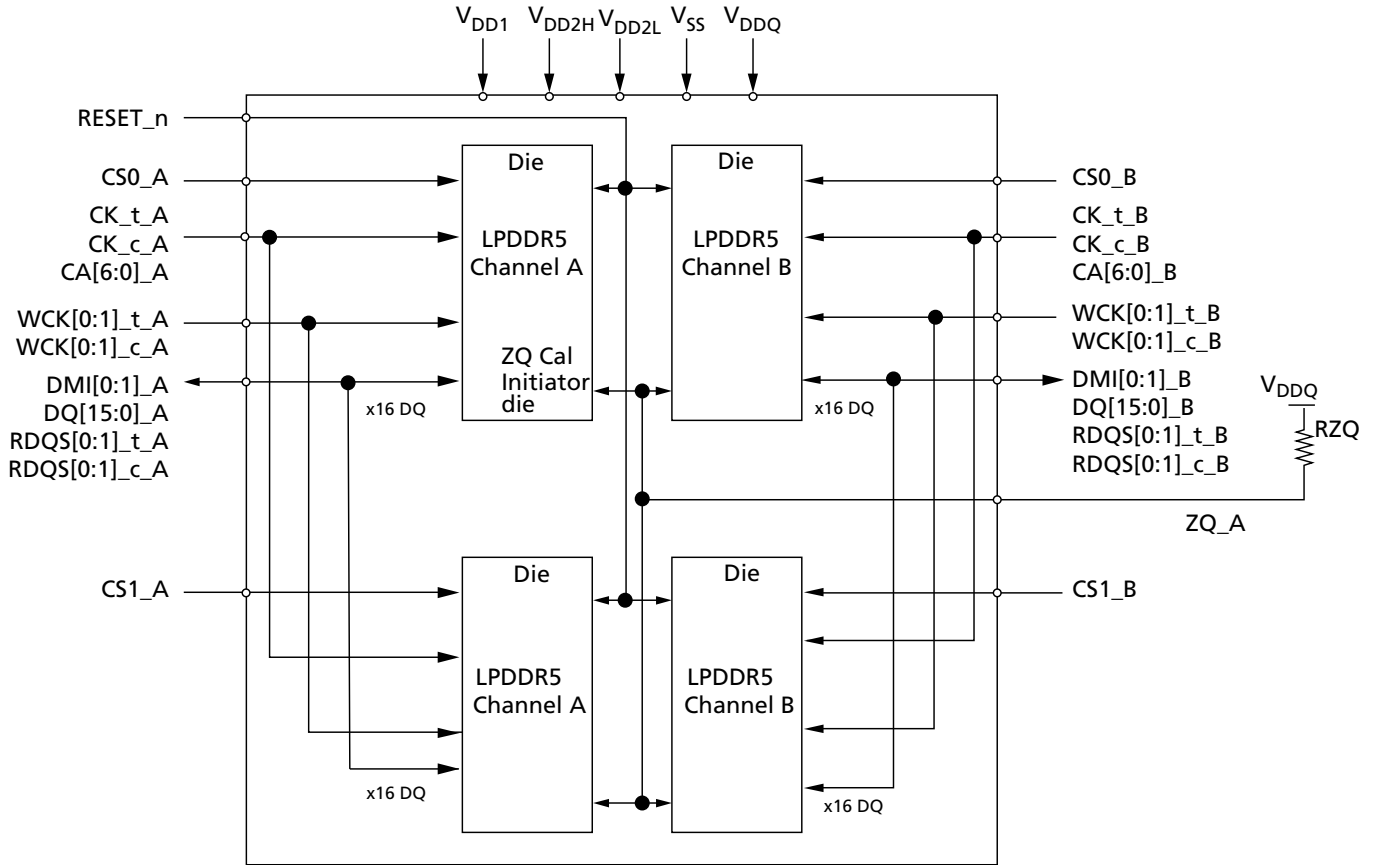




315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Package Block Diagrams

Quad Die, Dual Channel, Dual Rank

Figure 3: Quad Die, Dual Channel, Dual Rank Package Block Diagram

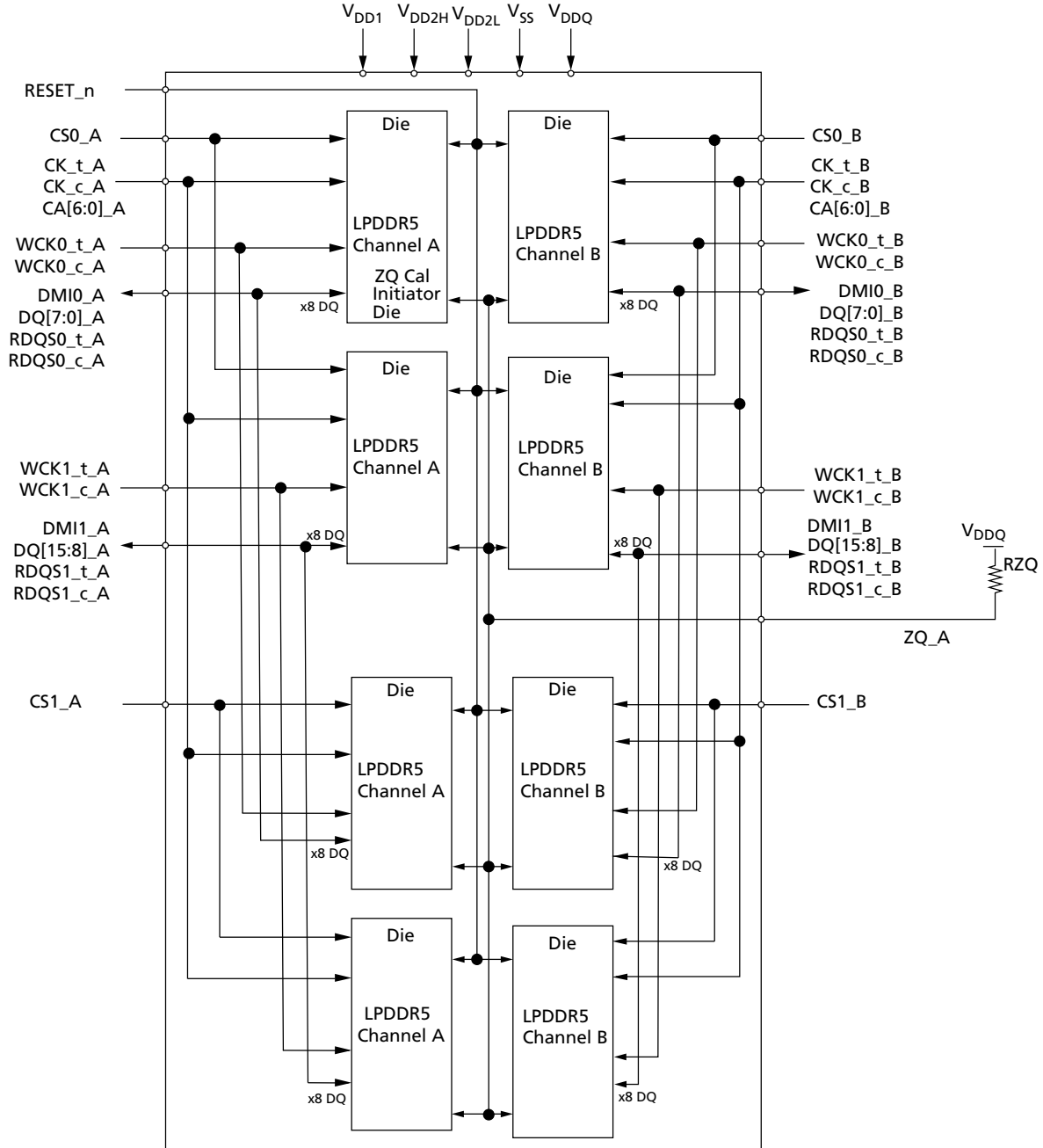




315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Package Block Diagrams

Eight Die, Dual Channel, Dual Rank

Figure 4: Eight Die, Dual Channel, Dual Rank Package Block Diagram





315b: x32 Automotive LPDDR5/LPDDR5X SDRAM 315b Dual Channel, 1 Rank, 2 Rank

315b Dual Channel, 1 Rank, 2 Rank

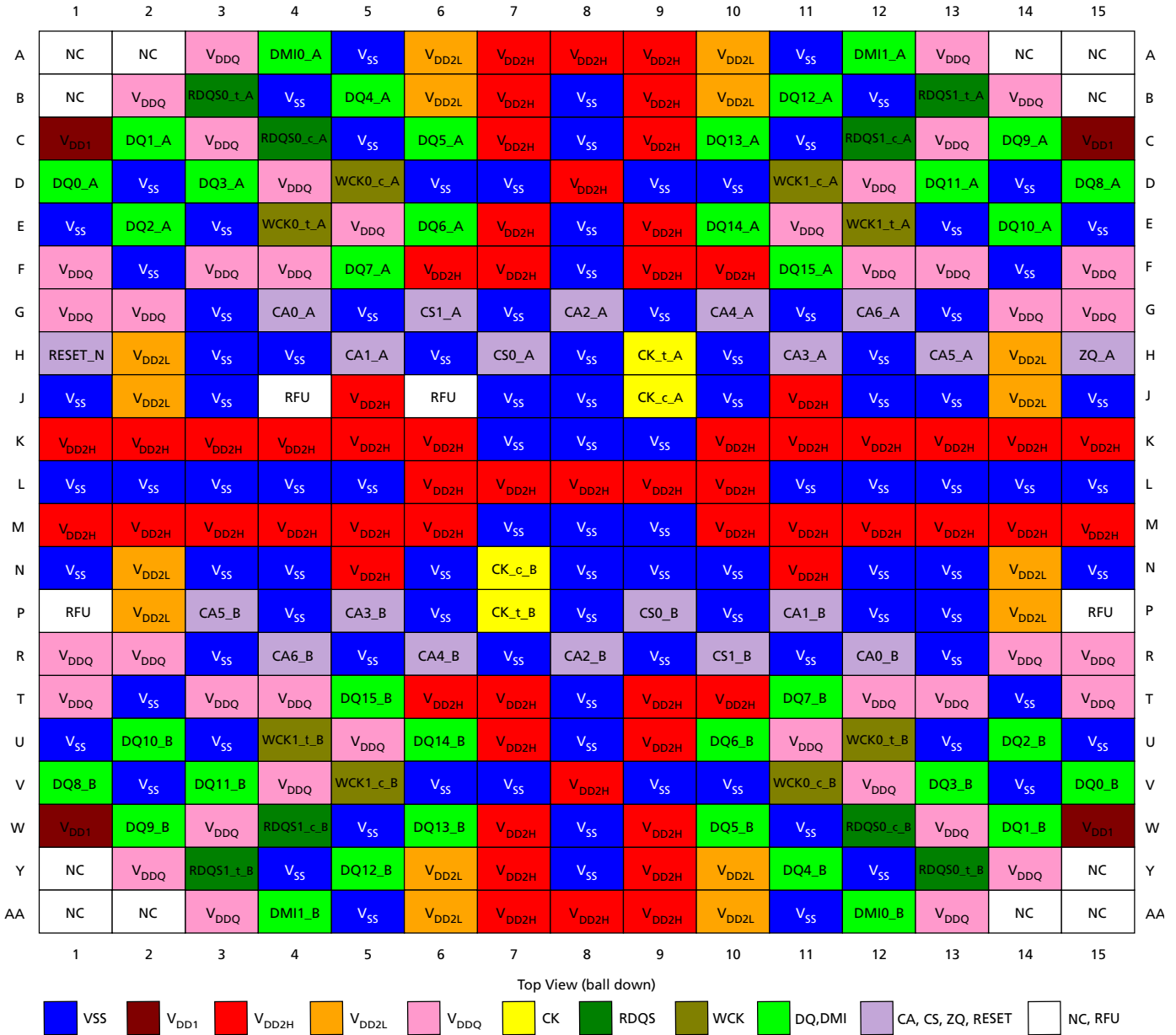
Table 5: 315-Ball/Pad Descriptions

Symbol	Type	Description
CK_t_[A:B], CK_c_[A:B]	Input	Clock: CK_t and CK_c are differential clock inputs. All double data rate (DDR) command/address inputs are sampled on both crossing points of CK_t and CK_c. The first crossing point is the rising (falling) edge of CK_t (CK_c) and second crossing point is falling (rising) edge of CK_t (CK_c). Single data rate (SDR) inputs, CS is sampled on the crossing point that is the rising (falling) edge of CK_t (CK_c).
CS0_[A:B], CS1_[A:B]	Input	Chip select: CS is part of the command code, and is sampled on the rising (falling) edge of CK_t (CK_c) unless the device is in power-down or deep sleep mode where it becomes an asynchronous signal. Each rank (0, 1) has its own CS signals. CS1_[A:B] become NC pins in a single-rank package.
CA[6:0]_[A:B]	Input	Command/address inputs: Provide the command and address inputs according to the command truth table.
WCK[1:0]_t_[A:B], WCK[1:0]_c_[A:B]	Input	Data clock: WCK_t and WCK_c are differential clock inputs used for write data capture and read data output.
DQ[15:0]_[A:B]	I/O	Data input/output: Bidirectional data bus.
RDQS[1:0]_t_[A:B], RDQS[1:0]_c_[A:B]	I/O Output	Read data strobe: RDQS_t and RDQS_c are differential output clock signals used to strobe data during a READ operation. RDQS_t is also used as a parity pin during write link protection enabled. Each byte of data has RDQS_t and RDQS_c signals.
DMI[1:0]_[A:B]	I/O	Data mask inversion: DMI serves multiple functions such as data mask (DM), data bus inversion (DBI), and parity at READ with ECC operation by setting the mode register. DMI is a bidirectional signal and each byte of data has a DMI signal.
ZQ_A	Reference	ZQ calibration reference: Used to calibrate the output drive strength and the termination resistance. The ZQ pin should be connected to V _{DDQ} through a 240Ω ±1% resistor.
V _{DDQ} , V _{DD1} , V _{DD2H} , V _{DD2L}	Supply	Power supplies: Isolated on the die for improved noise immunity.
V _{SS}	Supply	Ground reference: Power supply ground reference.
RESET_n	Input	Reset: When asserted LOW, the RESET pin resets the die. Reset is an asynchronous signal.
NC	–	No connect: Not internally connected.
RFU	–	Reserved Future Use: Not internally connected.



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM 315b Dual Channel, 1 Rank, 2 Rank

Figure 5: 315-Ball Dual-Channel Discrete FBGA



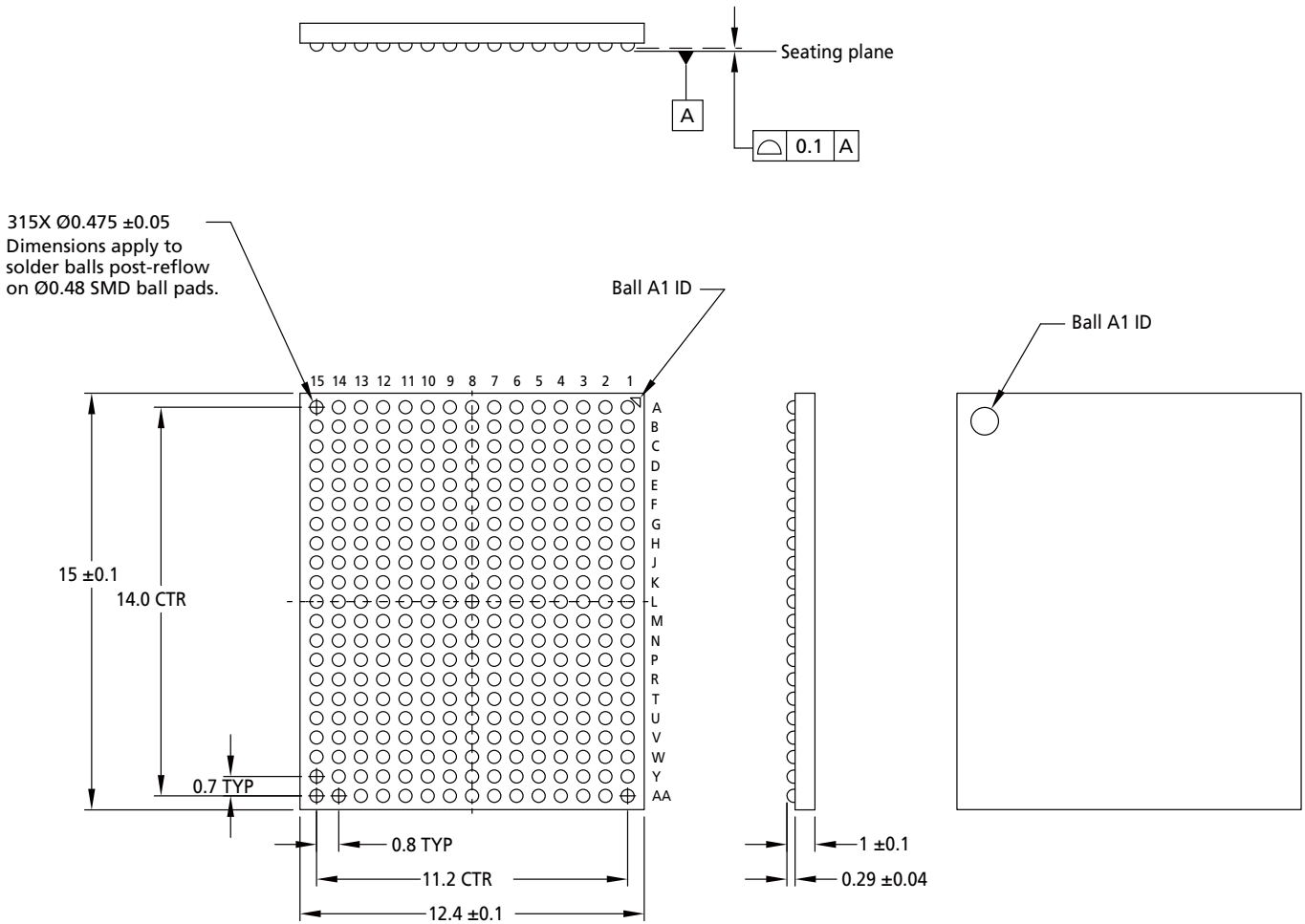


**315b: x32 Automotive LPDDR5/LPDDR5X SDRAM
Package Dimensions**

Package Dimensions

315-Ball Package (Package Code: DS)

Figure 6: 315-Ball TFBGA – 12.4mm (TYP) x 15.0mm (TYP) x 1.1mm (MAX)



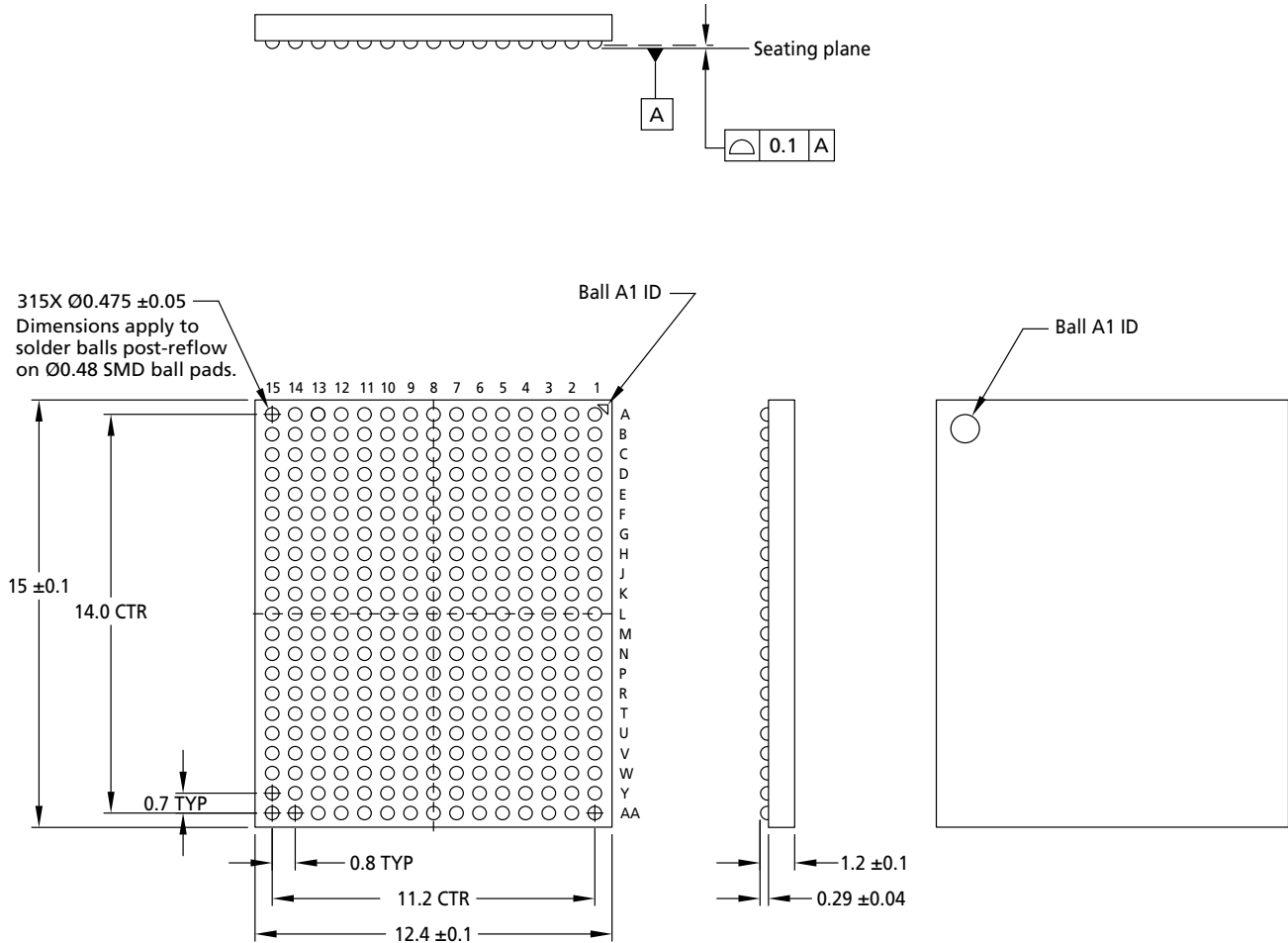
- Notes: 1. All dimensions are in millimeters.
2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Package Dimensions

315-Ball Package (Package Code: DV)

Figure 7: 315-Ball LFBGA – 12.4mm (TYP) x 15.0mm (TYP) x 1.3mm (MAX)



- Notes:
1. All dimensions are in millimeters.
 2. Solder ball composition: SACQ with CuOSP pads (Sn-4Ag-0.5Cu-3Bi-0.05Ni)



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Product-Specific Mode Register Definition

Product-Specific Mode Register Definition

Table 6: Mode Register Contents

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0	Per-pin DFE	Pre Emphasis	Unified NT ODT behavior mode	DMI output behavior mode	Optimized refresh mode	Enhanced WCK always-on mode	Latency mode	NT ODT timing mode
	OP[0] = 1b: Device supports different NT ODT latency for DQ and RDQS							
	OP[1] = 0b: Device supports x16 mode latency for 768M32, 1536M32 OP[1] = 1b: Device supports x8 mode latency for 3G32							
	OP[2] = 1b: Device supports enhanced WCK always-on mode							
	OP[3] = 1b: Device supports optimized refresh mode							
	OP[4] = 1b: Device supports both DMI behavior mode 1 and 2 and mode selection							
	OP[5] = 1b: The NT ODT behavior follows the unified NT ODT behavior							
	OP[6] = 1b: Device supports Pre Emphasis mode							
	OP[7] = 0b: Device does not support Per Pin DFE							
MR1							ARFM support ³	CS ODT OP support
	OP[0] = 0b: Device does not support CS ODT behavior OP							
	OP[1] = 0b: Device does not support ARFM							
MR3				BK/BG Org				
	OP[4:3] = 00b: BG, 01b: 8B, 10b: 16B Mode Supported							
MR5	Manufacturer ID							
	1111 1111b: Micron							
MR6	Revision ID1							
	0000 0111b							
MR8	I/O width		Density			Type		
	OP[7:6] = 00b: x16 for 768M32, 1536M32 OP[7:6] = 01b: x8 for 3G32		OP[5:2] = 0101b: 12Gb			OP[1:0] = 01b: LPDDR5X SDRAM		
MR13						VRO		
	OP[2] = 0b: Normal operation (default) 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR19			WCK2DQ OSC FM					
	OP[5] = 1b: WCK2DQ OSC FM supported							



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM Product-Specific Mode Register Definition

Table 6: Mode Register Contents (Continued)

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR21	WXS				ODTD-CSFS	WXFS	RDCFS	WDCFS
	OP[0] = 1b: WRITE DATA COPY function supported							
	OP[1] = 1b: READ DATA COPY function supported							
	OP[2] = 1b: WRITE X function supported							
	OP[3] = 1b: Device ODTD-CS is supported							
	OP[7] = 1b: Data to be written can be selected with 0 and 1							
MR22	RECC		WECC					
	OP[5:4] = 00b: Write link ECC disabled (default) 01b: Write link ECC enabled (See Note 4)							
	OP[7:6] = 00b: Read link ECC disabled (default) 01b: Read link ECC enabled (See Note 4)							
MR24	DFES				Read DCA			
	OP[3] = 1b: Device supports Read DCA							
	OP[7] = 1b: Device supports DFE							
MR26		RDQSTFS						
	OP[6] = 1b: Read/write-based RDQS_t TRAINING function supported							
MR27	RAAMULT		RAAIMT				RFM	
	OP[0] = 1b: RFM is required							
	OP[5:1] = 01110b: 112							
	OP[7:6] = 01b: 4X							
MR43		SBEC rule						
	OP[6] = 1b: Simultaneous SBE on each DQ byte and DMI are independently counted							
MR57	ARFM³				RFMSB	RAADEC		
	OP[1:0] = 10b: 2 × RAAIMT							
	OP[3:2] = 00b: 1 = Does not support single-bank mode							
	OP[7:6] = 00b: default (01110b: 112), 01b: Level A = 01101b: 104, Level B = 01100b: 96, Level C = 01011: 88							

- Notes: 1. The contents of mode registers described here reflect information specific to each die in these packages.
2. Refer to General LPDDR5/LPDDR5X Specification 1 for mode registers not described here.
3. Refer to General LPDDR5/LPDDR5X Specification 3 for feature description not described here.
4. Write link ECC and read link ECC are supported.



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM I_{DD} Parameters

I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section in General LPDDR5/LPDDR5X Specifications 2 for detailed conditions.

Table 7: I_{DD} Parameters at 7500 Mb/s – Single Die

Symbol	Supply	x8 7500 Mb/s			x16 7500 Mb/s			Unit	Note
		AIT	AAT	AUT	AIT	AAT	AUT		
I _{DD01}	V _{DD1}	3.3	3.3	3.6	3.3	3.3	3.6	mA	
I _{DD02H}	V _{DD2H}	29.5	29.5	34.5	30.0	30.0	35.0		
I _{DD02L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD0Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2P1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD2P2H}	V _{DD2H}	2.2	2.2	2.7	2.2	2.2	2.7		
I _{DD2P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2PS1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD2PS2H}	V _{DD2H}	2.2	2.2	2.7	2.2	2.2	2.7		
I _{DD2PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2N1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD2N2H}	V _{DD2H}	16.5	16.5	20.5	17.0	17.0	21.0		
I _{DD2N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2NS1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD2NS2H}	V _{DD2H}	16.5	16.5	20.5	17.0	17.0	21.0		
I _{DD2NS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3P1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD3P2H}	V _{DD2H}	6.0	6.0	8.0	6.0	6.0	8.0		
I _{DD3P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3PS1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD3PS2H}	V _{DD2H}	6.0	6.0	8.0	6.0	6.0	8.0		
I _{DD3PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM I_{DD} Parameters

Table 7: I_{DD} Parameters at 7500 Mb/s – Single Die

Symbol	Supply	x8 7500 Mb/s			x16 7500 Mb/s			Unit	Note
		AIT	AAT	AUT	AIT	AAT	AUT		
I _{DD3N1}	V _{DD1}	1.7	1.7	2.0	1.7	1.7	2.0	mA	
I _{DD3N2H}	V _{DD2H}	21.5	21.5	25.5	22.0	22.0	26.0		
I _{DD3N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3NS1}	V _{DD1}	1.7	1.7	2.0	1.7	1.7	2.0	mA	
I _{DD3NS2H}	V _{DD2H}	21.5	21.5	25.5	22.0	22.0	26.0		
I _{DD3NS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3NSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD4R1}	V _{DD1}	9.0	9.0	10.0	11.0	11.0	12.0	mA	3, 4
I _{DD4R2H}	V _{DD2H}	290.0	295.0	305.0	430.0	435.0	445.0		
I _{DD4R2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4RQ}	V _{DDQ}	58.0	58.0	58.0	116.0	116.0	116.0		
I _{DD4W1}	V _{DD1}	8.0	8.0	9.0	10.0	10.0	11.0	mA	3
I _{DD4W2H}	V _{DD2H}	200.0	205.0	215.0	280.0	285.0	295.0		
I _{DD4W2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4WQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD51}	V _{DD1}	17.0	17.0	17.0	17.0	17.0	17.0	mA	
I _{DD52H}	V _{DD2H}	115.0	115.0	120.0	115.0	115.0	120.0		
I _{DD52L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5AB1}	V _{DD1}	2.5	2.5	2.8	2.5	2.5	2.8	mA	
I _{DD5AB2H}	V _{DD2H}	23.5	23.5	27.5	24.0	24.0	28.0		
I _{DD5AB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5ABQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5PB1}	V _{DD1}	2.5	2.5	2.8	2.5	2.5	2.8	mA	
I _{DD5PB2H}	V _{DD2H}	23.5	23.5	27.5	24.0	24.0	28.0		
I _{DD5PB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5PBQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
 2. BG mode. DVFS and DVFSQ disabled.
 3. BL = 16, DBI disabled.
 4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
 5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V
 6. Notes 1 and 2 apply to entire table.



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM I_{DD} Parameters

Table 8: I_{DD} Parameters at 8533 Mb/s – Single Die

Symbol	Supply	x8 8533 Mb/s			x16 8533 Mb/s			Unit	Note
		AIT	AAT	AUT	AIT	AAT	AUT		
I _{DD01}	V _{DD1}	3.3	3.3	3.6	3.3	3.3	3.6	mA	
I _{DD02H}	V _{DD2H}	29.5	29.5	34.5	30.0	30.0	35.0		
I _{DD02L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD0Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2P1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD2P2H}	V _{DD2H}	2.2	2.2	2.7	2.2	2.2	2.7		
I _{DD2P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2PS1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD2PS2H}	V _{DD2H}	2.2	2.2	2.7	2.2	2.2	2.7		
I _{DD2PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2N1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD2N2H}	V _{DD2H}	16.5	16.5	20.5	17.00	17.0	21.0		
I _{DD2N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD2NS1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD2NS2H}	V _{DD2H}	16.5	16.5	20.5	17.0	17.0	21.0		
I _{DD2NS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD2NSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3P1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD3P2H}	V _{DD2H}	6.0	6.0	8.0	6.0	6.0	8.0		
I _{DD3P2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3PS1}	V _{DD1}	1.5	1.5	1.8	1.5	1.5	1.8	mA	
I _{DD3PS2H}	V _{DD2H}	6.0	6.0	8.0	6.0	6.0	8.0		
I _{DD3PS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3PSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD3N1}	V _{DD1}	1.7	1.7	2.0	1.7	1.7	2.0	mA	
I _{DD3N2H}	V _{DD2H}	21.5	21.5	25.5	22.0	22.0	26.0		
I _{DD3N2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3NQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM I_{DD} Parameters

Table 8: I_{DD} Parameters at 8533 Mb/s – Single Die

Symbol	Supply	x8 8533 Mb/s			x16 8533 Mb/s			Unit	Note
		AIT	AAT	AUT	AIT	AAT	AUT		
I _{DD3NS1}	V _{DD1}	1.7	1.7	2.0	1.7	1.7	2.0	mA	
I _{DD3NS2H}	V _{DD2H}	21.5	21.5	25.5	22.0	22.0	26.0		
I _{DD3NS2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD3NSQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD4R1}	V _{DD1}	10.0	10.0	11.0	12.0	12.0	13.0	mA	3, 4
I _{DD4R2H}	V _{DD2H}	320.0	325.0	335.0	480.0	485.0	495.0		
I _{DD4R2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4RQ}	V _{DDQ}	63.0	63.0	63.0	126.0	126.0	126.0		
I _{DD4W1}	V _{DD1}	9.0	9.0	10.0	11.0	11.0	12.0	mA	3
I _{DD4W2H}	V _{DD2H}	220.0	225.0	235.0	310.0	315.0	325.0		
I _{DD4W2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD4WQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD51}	V _{DD1}	17.0	17.0	17.0	17.0	17.0	17.0	mA	
I _{DD52H}	V _{DD2H}	115.0	115.0	120.0	115.0	115.0	120.0		
I _{DD52L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5Q}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5AB1}	V _{DD1}	2.5	2.5	2.8	2.5	2.5	2.8	mA	
I _{DD5AB2H}	V _{DD2H}	23.5	23.5	27.5	24.0	24.0	28.0		
I _{DD5AB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5ABQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		
I _{DD5PB1}	V _{DD1}	2.5	2.5	2.8	2.5	2.5	2.8	mA	
I _{DD5PB2H}	V _{DD2H}	23.5	23.5	27.5	24.0	24.0	28.0		
I _{DD5PB2L}	V _{DD2L}	0.2	0.2	0.2	0.2	0.2	0.2		
I _{DD5PBQ}	V _{DDQ}	0.6	0.6	0.6	0.6	0.6	0.6		

- Notes: 1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.
 2. BG mode. DVFS and DVFSQ disabled.
 3. BL = 16, DBI disabled.
 4. I_{DD4RQ} value is reference only. Typical value. Output load = 5pF; R_{ON} = 40 ohms; T_C = 25°C
 5. V_{DD1} = 1.70–1.95V; V_{DD2H} = 1.01–1.12V; V_{DD2L} = 0.87–0.97V; V_{DDQ} = 0.47–0.57V
 6. Notes 1 and 2 apply to entire table.



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM I_{DD} Parameters

Table 9: Full-Array Power-Down Self Refresh Current – Single Die

Temperature	Symbol	Supply	Value	Unit
25°C	I _{DD61}	V _{DD1}	0.25	mA
	I _{DD62H}	V _{DD2H}	0.45	
	I _{DD62L}	V _{DD2L}	(see note 4)	
	I _{DD6Q}	V _{DDQ}	(see note 4)	
	I _{DD6DS1}	V _{DD1}	0.25	
	I _{DD6DS2H}	V _{DD2H}	0.45	
	I _{DD6DS2L}	V _{DD2L}	(see note 4)	
	I _{DD6DSQ}	V _{DDQ}	(see note 4)	
95°C	I _{DD61}	V _{DD1}	3.70	mA
	I _{DD62H}	V _{DD2H}	12.00	
	I _{DD62L}	V _{DD2L}	0.20	
	I _{DD6Q}	V _{DDQ}	0.60	
	I _{DD6DS1}	V _{DD1}	3.70	
	I _{DD6DS2H}	V _{DD2H}	12.00	
	I _{DD6DS2L}	V _{DD2L}	0.20	
	I _{DD6DSQ}	V _{DDQ}	0.60	
105°C	I _{DD61}	V _{DD1}	4.00	mA
	I _{DD62H}	V _{DD2H}	17.00	
	I _{DD62L}	V _{DD2L}	0.20	
	I _{DD6Q}	V _{DDQ}	0.60	
	I _{DD6DS1}	V _{DD1}	4.00	
	I _{DD6DS2H}	V _{DD2H}	17.00	
	I _{DD6DS2L}	V _{DD2L}	0.20	
	I _{DD6DSQ}	V _{DDQ}	0.60	
125°C	I _{DD61}	V _{DD1}	7.00	mA
	I _{DD62H}	V _{DD2H}	36.00	
	I _{DD62L}	V _{DD2L}	0.20	
	I _{DD6Q}	V _{DDQ}	0.60	
	I _{DD6DS1}	V _{DD1}	7.00	
	I _{DD6DS2H}	V _{DD2H}	36.00	
	I _{DD6DS2L}	V _{DD2L}	0.20	
	I _{DD6DSQ}	V _{DDQ}	0.60	



315b: x32 Automotive LPDDR5/LPDDR5X SDRAM I_{DD} Parameters

- Notes:
1. $I_{DD6}^{25^{\circ}\text{C}}$ is the typical value in the distribution with nominal V_{DD} and a reference-only value. $I_{DD6}^{95/105/125^{\circ}\text{C}}$ is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.
 2. DVFS and DVFSQ disabled.
 3. $V_{DD1} = 1.70\text{--}1.95\text{V}$; $V_{DD2H} = 1.01\text{--}1.12\text{V}$; $V_{DD2L} = 0.87\text{--}0.97\text{V}$; $V_{DDQ} = 0.47\text{--}0.57\text{V}$
 4. V_{DD2L} and V_{DDQ} power rails are not used during power-down self refresh.